What is claimed is:

1. A circuit board having a boundary scan self-testing function, comprising:

a substrate;

a plurality of devices under test mounted on the substrate and having boundary scan circuits; and

an active testing device mounted on the substrate and used for generating boundary scan testing data sequentially forwarding to the devices under test along a testing route.

2. The circuit board having a boundary scan self-testing function of Claim 1, wherein the devices under test include programmable devices.

3. The circuit board having a boundary scan self-testing function of Claim 2, wherein the programmable devices are complex programmable logic devices or field programmable gate array devices.

4. The circuit board having a boundary scan self-testing function of Claim 1, wherein the active testing device includes TCK, TMS and TRST pins which connect the devices under test in parallel, and further includes TDI and TDO pins which connect the devices under test in series.

5. The circuit board having a boundary scan self-testing function of Claim 1, wherein the substrate further includes at least one I/O port for outputting test results of the active testing device.

6. The circuit board having a boundary scan self-testing function of Claim 4, wherein the substrate includes test access ports having a short circuit between the TDI and TDO pins.

7. The circuit board having a boundary scan self-testing function

of Claim 2, wherein the active testing device has program codes of the programmable devices, which can be written into the programmable devices through the testing route.